

# Mohamed Ismail Bari

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Nationality: Indian

UK work status: **HSMP visa valid until Nov 2011**

Current Notice period: Contact me and ask

Willing to relocate: Yes

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## OBJECTIVE

To obtain a senior position in electrical engineering that utilizes my seven years of experience in the following areas - electronic system design, electrical modeling and package design, EMI, EMC, product reliability, and my bachelors' degree in electronics and communication.

## EDUCATION

Bachelor of Engineering (BE Electronics & Communication) 1997 – 2001  
Bharathiyar University, India

## PROFESSIONAL EXPERIENCE

Period	Company Name	Designation	Field of Work
Aug 2005 – Present	SCM Microsystems (India)	Senior Hardware Engineer	Smart card reader design and development
Dec 2003 – Aug 2005	Intel Corporation (India)	Component Design Engineer	Power Delivery Electrical Analysis /Package design
Jul 2001 – Dec 2003	HCL Technologies (India)	Member Technical Staff	Board Design/FPGA

## KEY STRENGTHS

- Good signal integrity analysis skills
- Strong team player
- Highly proficient in C, C++, Visual C++, Assembly language.
- Good circuit designing capability.
- Good analytical skills.
- Knowledge of EMI, EMC and reliability concepts.
- Comfortable with most of the PCB/Schematic design tools.

### Project lead – RFID reader design and development

**SCM Microsystems**, Chennai, India ([www.scmmicro.com](http://www.scmmicro.com))

**Clients** : Datacard, 3M, Zebra

**Travel** : Berlin (inter-operability show)

Singapore, Indonesia (Mass production)

SCM Microsystems develops hardware and system solutions that enable people to conveniently and securely access digital content and services. The Company offers a range of smart card-based solutions and digital media readers to the worldwide photo kiosk market. The company is also one of the pioneers in RFID and epassport readers. My responsibilities include the following.

### Skills:

#### Programming:

C, C++, Visual Basic, Visual C++

#### Tools :

HSPICE, PSPICE  
Orcad 9.2, PCAD 2002,  
Protel 99SE, Allegro 14.0,  
Spectra 13.0, Ansoft  
3D/2D 5.0,  
Ansoft Links 2.2,  
APD 14.0 Package Layout

#### Protocols:

PCI, ISA, I2C, SPI, RS485,  
JTAG, USB, TCP/IP

#### Equipments:

Oscilloscopes, Logic Analyzer, Impedance Analyzer

### Duration:

Sept 2005 – Present

- Overall hardware design for Contact and Contactless (13.56MHz) smartcard/RFID readers using 8051 based USB microcontrollers
- Managing and mentoring a team of three junior electronics engineers
- End-to-end responsibility for two Contactless smartcard reader product lines
- Liaising with cross-functional teams for effective product mass production.
- Analog/Digital circuit design, Schematic design, PCB layout guidance, Component selection/approval, BOM preparation and preparation of production guidelines for mass production
- Product FCC, CE and UL certifications
- RMA analysis and hardware debugging

### **RFID Dual Antenna ePassport Reader**

**Duration :** Jan '07 – Jul '07

**Travel :** U.S.A, Boston

**Client :** Viisage, L1 identification

This project is a ePassport reader (13.56MHz) incorporating two reader antennae close to each other. The greatest challenge in this design is to avoid inter-antenna coupling between the two antennae. To avoid inter-antenna coupling, a shorting mechanism was implemented where the inactive antenna will be electrically detuned when the other antenna is active.

- Hardware design and software development support
- Project management and defect tracking
- Realized a working prototype and delivered it to the customer
- Sign-off from the customer for proceeding with the mass production

### **Handheld RFID Reader – TAN Generator**

**Duration :** Oct '06 – Dec '06

**Travel :** None

**Client :** MasterCard

This project is a handheld, battery operated, Contactless (13.56MHz) reader used for Transaction Access Number (TAN) generation. The greatest challenge was on the low power design as the device operates on two AA batteries. Further, the project had a very aggressive timeline. I successfully completed this project within an aggressive timeline.

- Hardware design from the scratch using Samsung microcontroller (S3C826A)
- Coordinated the firmware design with a German consultant
- Project management and defect tracking
- Realized a working prototype within a short time (21 days)

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### **Component Design Engineer**

**Intel Corporation**, Bangalore, India ([www.intel.com](http://www.intel.com))

Intel is the world leader in silicon innovation, develops processor technologies and supports global technology initiatives.

I performed power delivery analysis for Intel's latest microprocessors. HSPICE was used to electrically model the microprocessor I/O interface and core interfaces. The goal is to ensure efficient power delivery even under worst-case transient switching. Based on simulations results, appropriate recommendations were

***Duration:***

Dec 2003 – Sept 2005

provided to the design teams on the amount of on-die, on-package and motherboard capacitance required to meet the targeted noise margin.

- To make package design/layout recommendations and sustain power supply noises in the microprocessor
- To recommend the amount of capacitance needed on the processor die, on the package and on the motherboard.
- Electrical modeling and analysis of package and processor die using HSPICE tool
- Provide design recommendations to package and circuit design team
- Developed an in-house tool using Visual C++ for easy electrical modeling of the transient load

### **Whitefield Network Processor – Power delivery analysis**

**Duration :** Dec '03 – Dec '04

**Travel :** USA

### **Tukwila Network Processor – Power delivery analysis**

**Duration :** Jul'04 – Jun '05

**Travel :** None

- Electrical modeling and analysis of package and processor die in HSPICE.
- Worked with cross-functional teams to acquire the necessary inputs for setting up the simulation deck.
- Provided recommendations on the amount of capacitance required at each level of the power delivery network (viz, on-die, on-package and on motherboard till the SMPS).

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### **Member Technical Staff**

**HCL Technologies**, Chennai, India ([www.hcltech.com](http://www.hcltech.com))

HCL Technologies is a leading global IT services company in India providing a wide range of services to its clients. The hardware division is one of the best in industry have a broad range of expertise on development of medical electronics to avionics systems.

I performed as a technical staff responsible for hardware design and development. Assisted the senior members extensively during the design phase till the board bring-up stage.

### **Optical Fiber Channel (FC) Simulator**

**Duration :** Oct'03 – Dec '03

**Travel :** None

**Client :** McData, Colorado, USA

The primary objective of this project is to develop a PCI based add-on card. The hardware is used to send FC data over optical fiber at a data rate of 10Gbps. However, the hardware also supports 1Gbps, 2Gbps and 4Gbps. Most of the functionality is implemented in software. The hardware just transmits/receives the FC data and presents it to the higher layers.

- Assisted in Overall design
- Component Selection
- Schematics design and layout guidance

### ***Tools Used :***

Synopsys HSPICE, Cougar V2.8.1, AvanWaves, Ansoft Q3D 5.0, Ansoft 2D 5.0, Ansoft Links 2.2, APD 14.0 (Package Design)

### ***Duration:***

Jul 2001 – Dec 2003

### ***Tools Used :***

Mentor Board Station, Modelsim 5.0, Synplify pro 5.1, Xilinx Foundation series

## Ethernet / LAC / OEB Interface Board Design

**Duration :** Nov '02 – Sept '03

**Travel :** California, U.S.A

**Client :** Rockwell Collins passenger systems, California, U.S.A

The eTES Area Distribution Box (eADB) is part of the eTES In-Flight Entertainment System. This is a Motorola MP860T based card. The eADB forms the backbone of the IFE Cabin Distribution Network for Boeing and Airbus line airplanes, and for retrofit applications on in-service Boeing and Airbus aircrafts.

- Overall architecture design for hardware
- Designed power sequencing circuits
- Developed schematics
- Performed analog circuit analysis and simulations
- Assisted PCB component placement and routing
- Developed diagnostics for board validation in C language
- Performed board bring-up at onsite
- Assisted in EMI testing
- Assisted in board manufacturing and in procuring components

## Network Processor based Line Card for Ethernet over VDSL

**Duration :** Jun '02 - Oct '02

**Travel :** None

**Client :** Accordion Networks, California, U.S.A

Designed and developed a board for Ethernet-over-VDSL communication. The board uses INTEL Network Processor (IXP1200) for processing and transmitting VDSL packets received from the VDSL end through the INTEL IXP440 MAC (100 Mbps) to the back plane. The back plane consists of a cross-stream switch fabric (Vitesse VSC870 – VSC880) for switching the packets to other line cards.

- Prepared system requirements document
- Prepared High level design document
- Identified required components
- Calculated overall power budget
- Developed Schematics and PCB review
- Guided component placement and routing.
- Signal integrity analysis using IBIS models
- Performed board bring up at the offshore facility

## OC-48 I/O Board Design

**Duration :** Dec '01 – May'02

**Travel :** None

**Client :** IPolicy Networks, California, U.S.A

This board design was intended to convert FOCUS bus (Vitesse proprietary bus) signals to OC-48 optical signals. The design consists of two channels of optical communication where two FPGA devices were used. The data signal from the FOCUS bus was converted into POS-PHY level 3 signals by the FPGA. Thereafter, the POS-PHY signal was processed by the optical framer/mapper (VSC9142), which converts the electrical signal to optical signal. Since data rate was very high, signal integrity analysis was done for routing the signals.

- Prepared High-level design document
- Identified required components
- Calculated overall power budget

### ***Tools Used :***

NC VHDL, Modelsim  
PCAD 2001 Schematic,  
PCAD 2001 PCB layout,  
Spectra – Auto routing,  
Microware OS9 builder –  
OS9000 application  
builder,  
Simetrix 4.1c – Circuit  
simulation,  
PVCS – Version control  
system,  
PVCS Tracker – Bug  
Tracking system

### ***Tools Used :***

Orcad 9.25,  
Allegro v14.0, SigXplorer –  
Signal Integrity analysis  
tool  
Spectra – Auto routing  
tool  
Winriver VxWorks  
Compiler – For building  
diagnostics bundle with  
the Board Support  
Package (BSP).  
PVCS – Version control  
system  
PVCS Tracker – Bug  
Tracking system

### ***Tools used :***

Orcad 7.1.25,  
Allegro v13.0,  
SigXplorer – Signal  
Integrity analysis tool,  
Spectra,  
PVCS – Version control  
system,  
PVCS Tracker – Bug  
Tracking system

- Created schematics symbols
- Developed schematics
- Integrated schematics
- Reviewed PCB symbols
- Guided component placement and routing.
- Collected IBIS models for signal integrity analysis
- Analyzed signal quality for critical signals using IBIS models and sigexplorer (Signal Integrity)
- Signal Integrity report generation

### **POS PHY Level-3 Bus to FOCUS Bus Bridge FPGA**

**Duration :** Jul '01 – Nov '01

**Travel :** None

**Client :** Vitesse Semiconductors, California, U.S.A

The FPGA converts POS-PHY level 3 bus signals to FOCUS bus signals and vice versa. FOCUS bus is a proprietary bus used in Vitesse semiconductors in their network processor product line. The FPGA is intended to seamlessly integrate the POS-PHY bus to the FOCUS bus at a data rate of 100Mbps.

- Design and coding one of the modules in the FPGA
  - Validated the entire design on silicon
  - Successfully validated the design at 100 MHz
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#### ***Tools used :***

Synplify 5.1 – FPGA  
synthesis tool,  
Xilinx Foundation Series 4,  
PVCS – Version control  
system,  
PVCS Tracker – Bug  
Tracking system